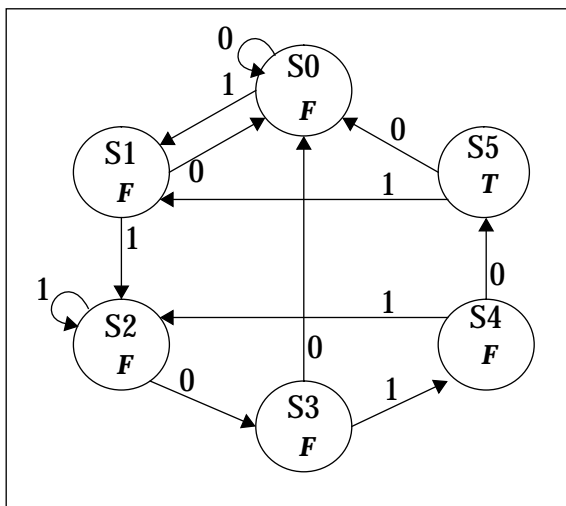


HOMWORK

ASSIGNMENT #2

Due Date: Thursday, February 19, 1997

- Implement the Finite State Machine below that detects the bit sequence 1 1 0 1 0



- Use an enumerated type to define the states.
- The STD_LOGIC state machine clock is *clkIn*.
- The STD_LOGIC state machine ASYNCHRONOUS reset is *resetLowIn*.
- The BIT data input is *dataIn*.
- The BOOLEAN FSM output is *detectTrueOut* and is one clock period in duration.

- **Write** a process for a *registered output* implementation (see Slide 146 in CourseNotes.)
- **Simulate** the FSM and use the simulator to apply a clock and reset.
- ◇ **Turn in** a Hardcopy of your code and the waveform traces for all signals.
- ◇ **Turn in** your Code via E-mail.

***** Please include your name and Student ID number on all homework submissions *****