Course Outline and Policies

ECE 496B / 596B - Digital Systems Design with VHDL

Spring 1998

Instructor: David M. Clark
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Raytheon Systems Company

Office: TBD
Telephone: TBD

Class Hours: Tues. / Thurs. 5:00-6:15 pm
Class Location: ECE 102

Office Hours: Tues. / Thurs. 6:15-7:15 pm (after class)

Text Book: VHDL for Programmable Logic, Kevin Skahill
Addison-Wesley Publishers

Other Materials: Course Notes

Prerequisites: Digital Design
High-level programming language

Equipment: In order to run the required design tools (*Cypress Warp 2* VHDL Compiler for PLDs), students will be required to have their own access to a Personal Computer with the following system requirements:

- IBM PC or equivalent (486 or higher recommended)
- 16 MBytes of RAM (32 MBytes recommended)
- 35 MBytes hard disk space
- CD-ROM drive
- Windows 3.1x, Windows 95, or Windows NT
- 3.5” floppy disk drive

Coursework: There will be homework due, both written problems and those that require lab work (coding, simulation, synthesis)

595B students will in many cases be required to demonstrate a higher degree of understanding of the associated material through more complex or extended work -- details will accompany each assignment.

Final Project: There will be a moderate design project required that will entail coding, simulation, and synthesis. The project will consist of design work and a written project report.

596B students will be required to demonstrate a higher degree of expertise. In particular, they will be required to generate a written simulation plan for the project as well as code formal stimulus and response modules to implement the simulation plan to test the functionality of the project device-under-test -- details will accompany the project assignment handout.

Grading: Undergraduate and Graduate students will be graded separately, and the groups will be individually "curved" as appropriate.

The grade contributions are:

25% Homework Exercises / Lab Work

25% Midterm

25% Project

25% Final

No late homework will be accepted.

Plagiarism and copying will not be tolerated. Students are expected to do their own work. Students obtaining more than basic assistance for homework(s) and/or the project must acknowledge the source. Students must not accept substantial assistance from any party -- consult the instructor if significant assistance is required.

Syllabus

ECE 496B / 596B - Digital Systems Design with VHDL

1. Introduction

Course scope and an answer to the question "What is VHDL?"

2. Language Overview

Basic introduction of the various constructs and elements of the language to facilitate hands-on laboratory work as early as possible, including how to invoke and use the design tools

3. Language Elements

Predefined data types, user data types, signals, operators

4. Concurrence

The concurrent nature of VHDL, how it represents real hardware, and how to use the language to implement concurrent hardware, including processes, concurrent signal assignments, variables

5. Sequential Statements

Control structures and sequential flow within concurrent code regions, such as IF...ELSIF...ELSE, looping, CASE

6. Common Design Constructs

Many commonly encountered design constructs and their VHDL counterparts, including Finite State Machines, counters, externally programmable registers, multiplexers, tri-state busses, latches and edge-triggered flip-flops

7. Design Units

In-depth discussion of design hierarchy, such as entities, architectures, packages, libraries, component instantiation, and configurations

8. Advanced Topics

Subprograms, overloading, scope and visibility, blocks, generate statements, generics, resolution functions, implication versus inference

9. Design Example

A sizable design will be created interactively in VHDL, demonstrating how to partition a design for VHDL, how to formulate relevant data types, and introducing and using various stylistic elements to promote code reuse and maintainability

10. Testbench

Various topics regarding testbench generation and modeling, including driver and receiver modules, physical types, files and text i/o, and assert statements

11. Testbench Example

A testbench will be created interactively in VHDL to provide automated stimulus and results checking for the earlier Design Example created in class

12. Synthesis

Using design tools to synthesize VHDL code into logic gates